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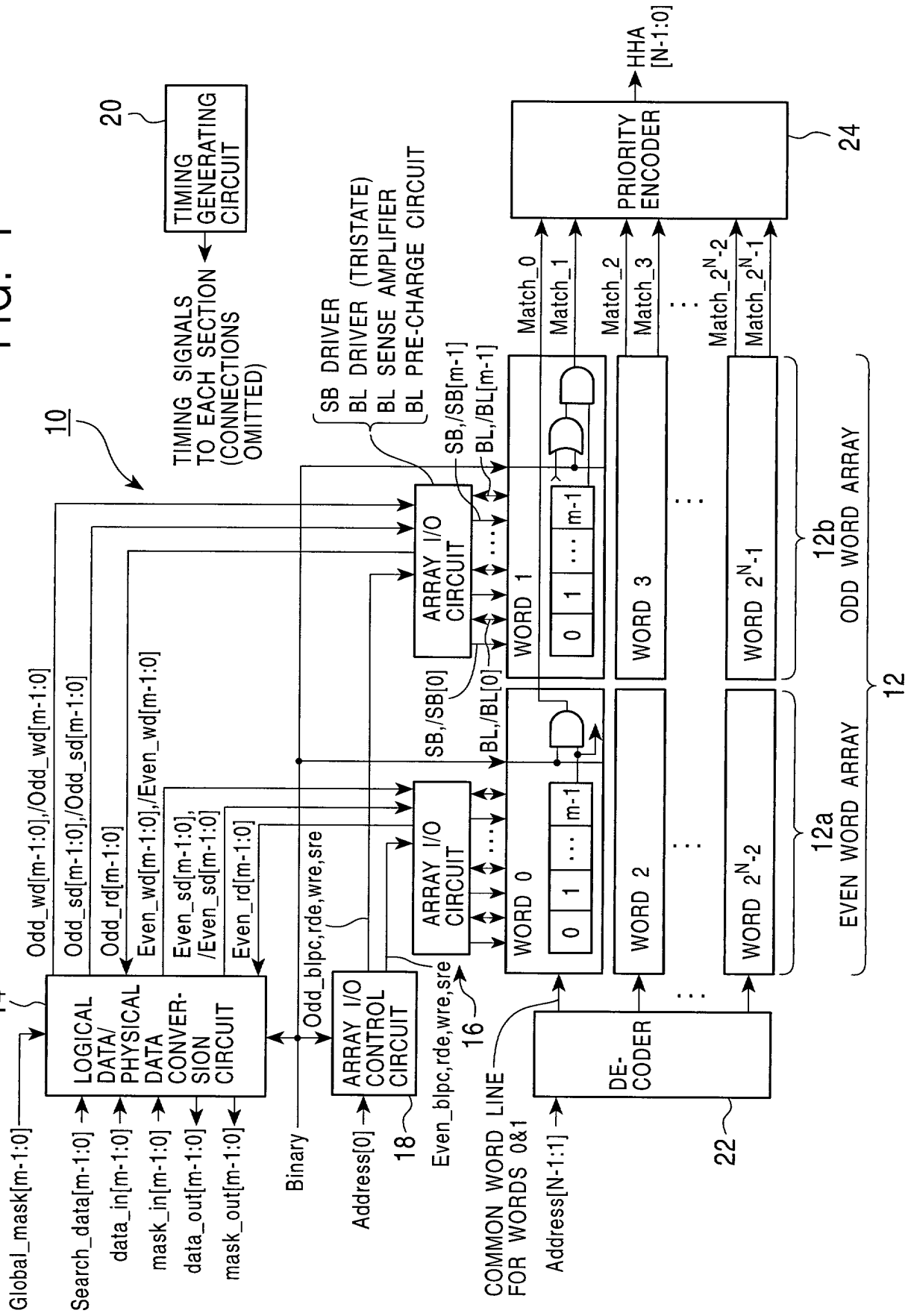


FIG. 2

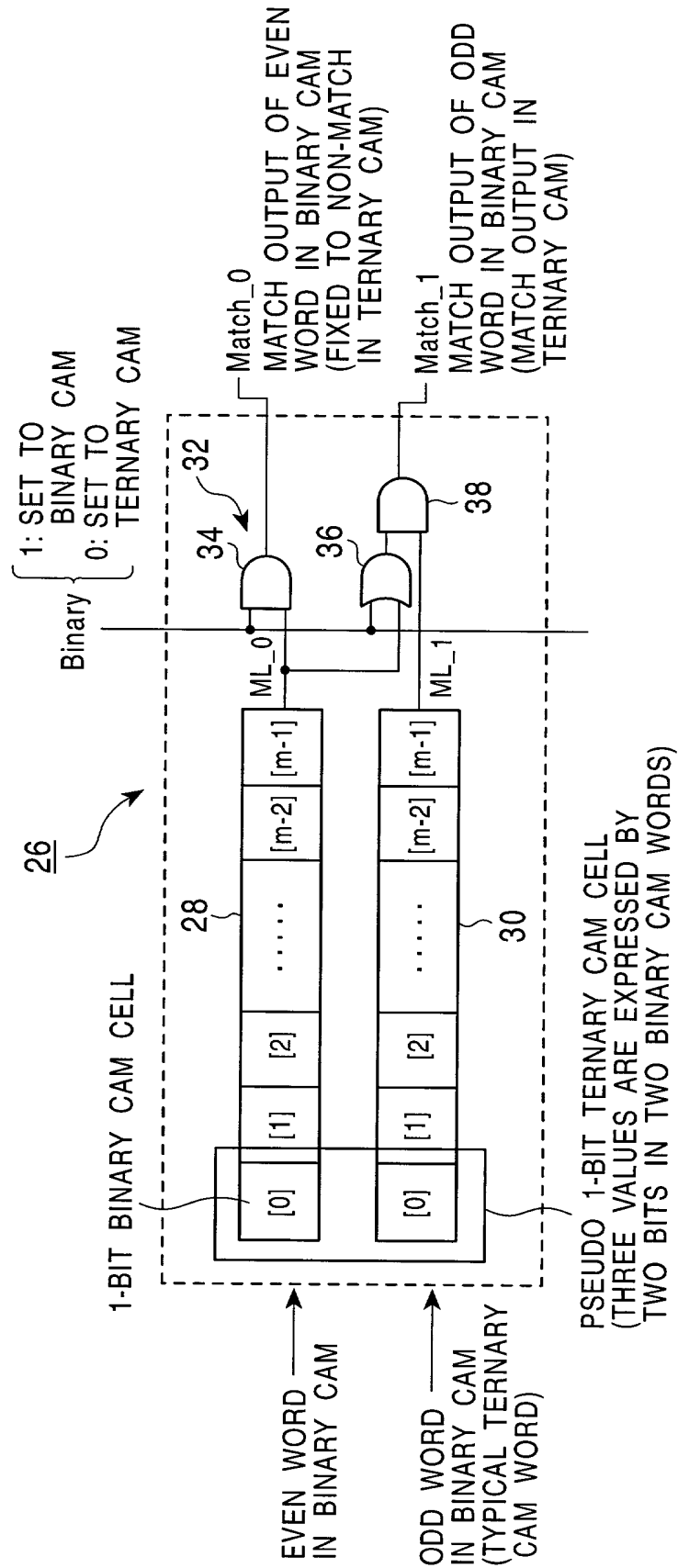


FIG. 3

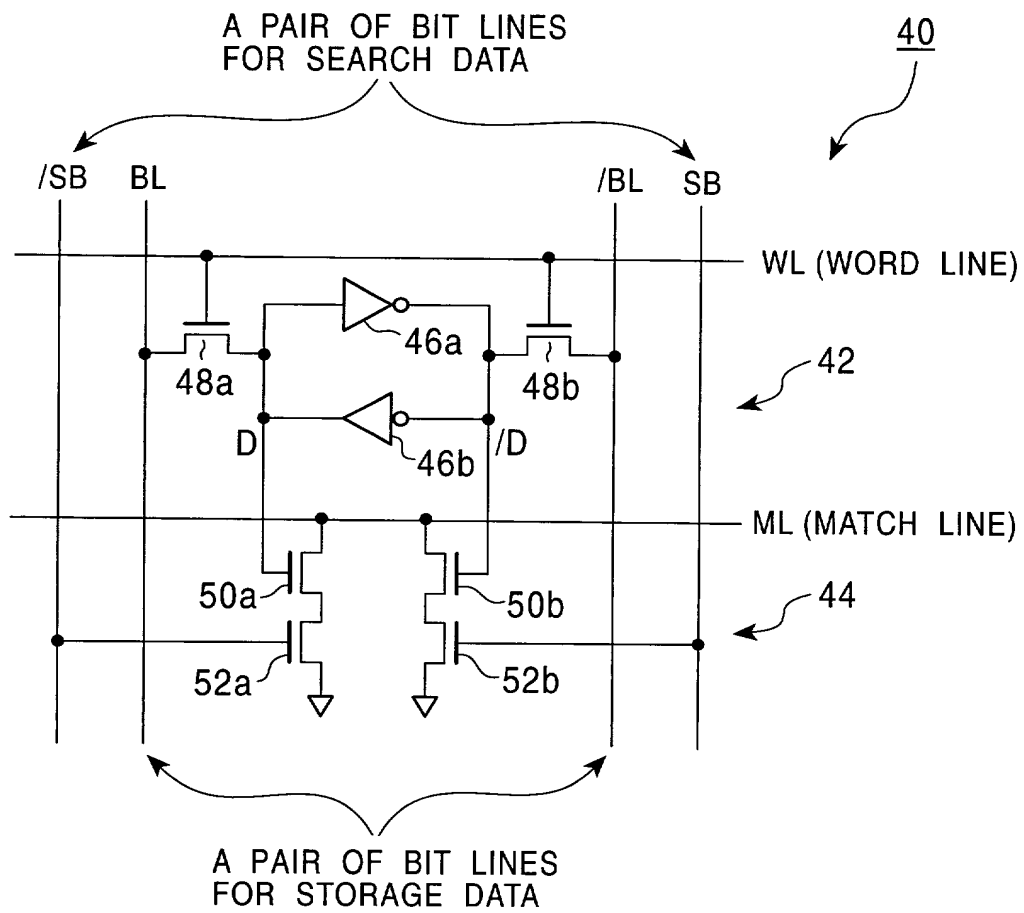


FIG. 4A

LOGICAL DATA	PHYSICAL DATA	SEARCH DATA	SEARCH BIT LINE OUTPUTS (SB/SB)
0	0	0	0 DRIVEN (0,1)
1	1	1	1 DRIVEN (1,0)
		DON'T CARE	DON'T CARE (0,0)

FIG. 4B

EXTERNAL DATA	LOGICAL DATA (CONVENTIONAL TERNARY CAM DATA)		PHYSICAL DATA (INTERNAL DATA OF PRESENT INVENTION)		SEARCH DATA	SEARCH BIT LINE OUTPUTS (SB/SB)	
	STORAGE DATA	MASK DATA	EVEN CELL	ODD CELL		EVEN	ODD
0	0	0	0	0	0	DON'T CARE (0,0)	0 DRIVEN (0,1)
1	1	0	1	1	1	1 DRIVEN (1,0)	DON'T CARE (0,0)
DON'T CARE	X (UNDEFINED)	1	1	0	DON'T CARE	DON'T CARE (0,0)	DON'T CARE (0,0)

FIG. 5A

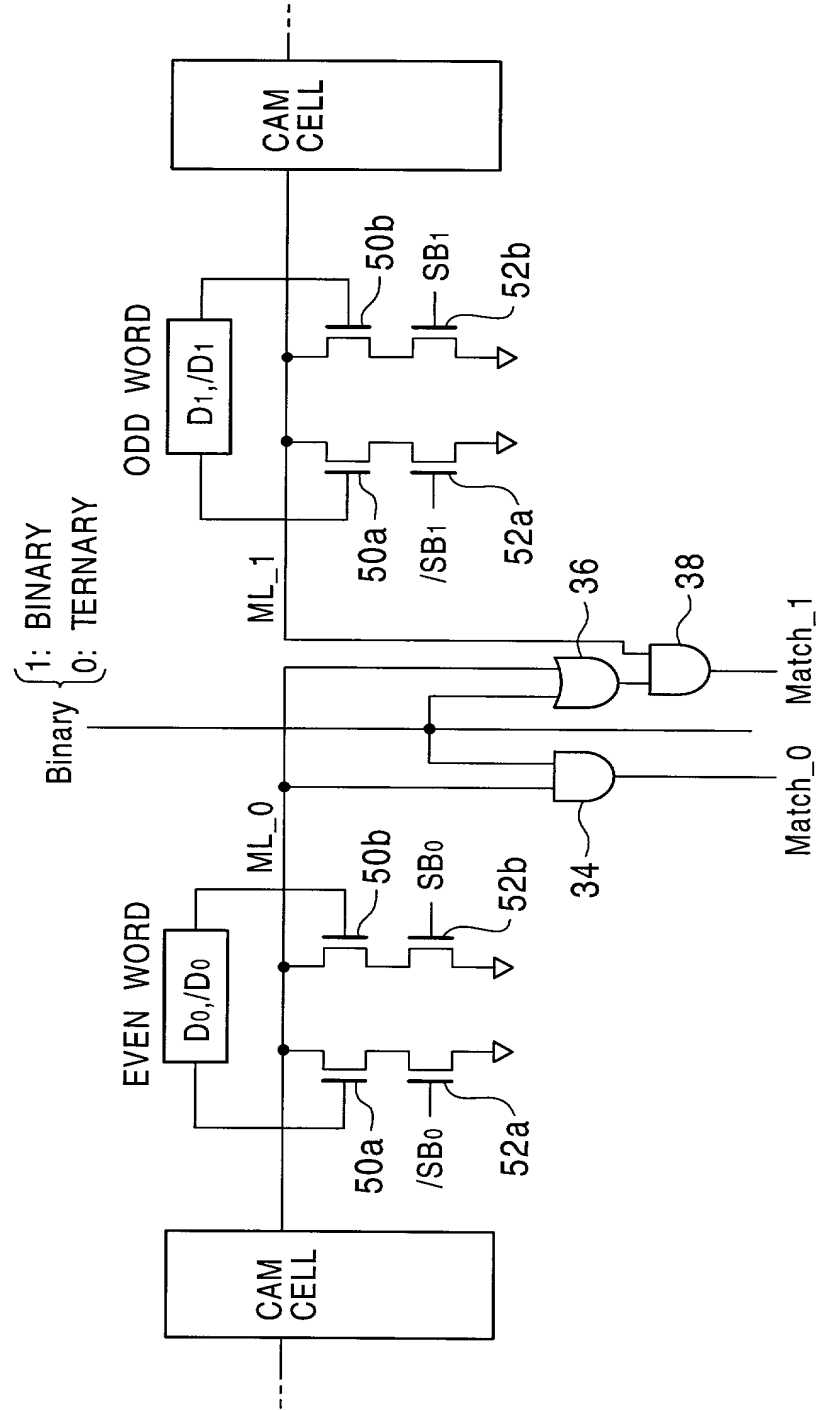


FIG. 5B

STORAGE DATA		SEARCH DATA			ML_0	ML_1	Match_0	Match_1
DATA	EVEN (D <sub>0</sub> )	ODD (D <sub>1</sub> )	DATA	EVEN (SB <sub>0</sub> /SB <sub>0</sub> )	ODD (SB <sub>1</sub> /SB <sub>1</sub> )			
0	0	0	0	(0,0)	(0,1)	1	0	1
			1	(1,0)	(0,0)	0		0
			X	(0,0)	(0,0)	1		1
1	1	1	0	(0,0)	(0,1)	1	0	0
			1	(1,0)	(0,0)	1		1
			X	(0,0)	(0,0)	1		1
X	1	0	0	(0,0)	(0,1)	1	0	1
			1	(1,0)	(0,0)	1		1
			X	(0,0)	(0,0)	1		1

X: DON'T CARE

FIG. 6

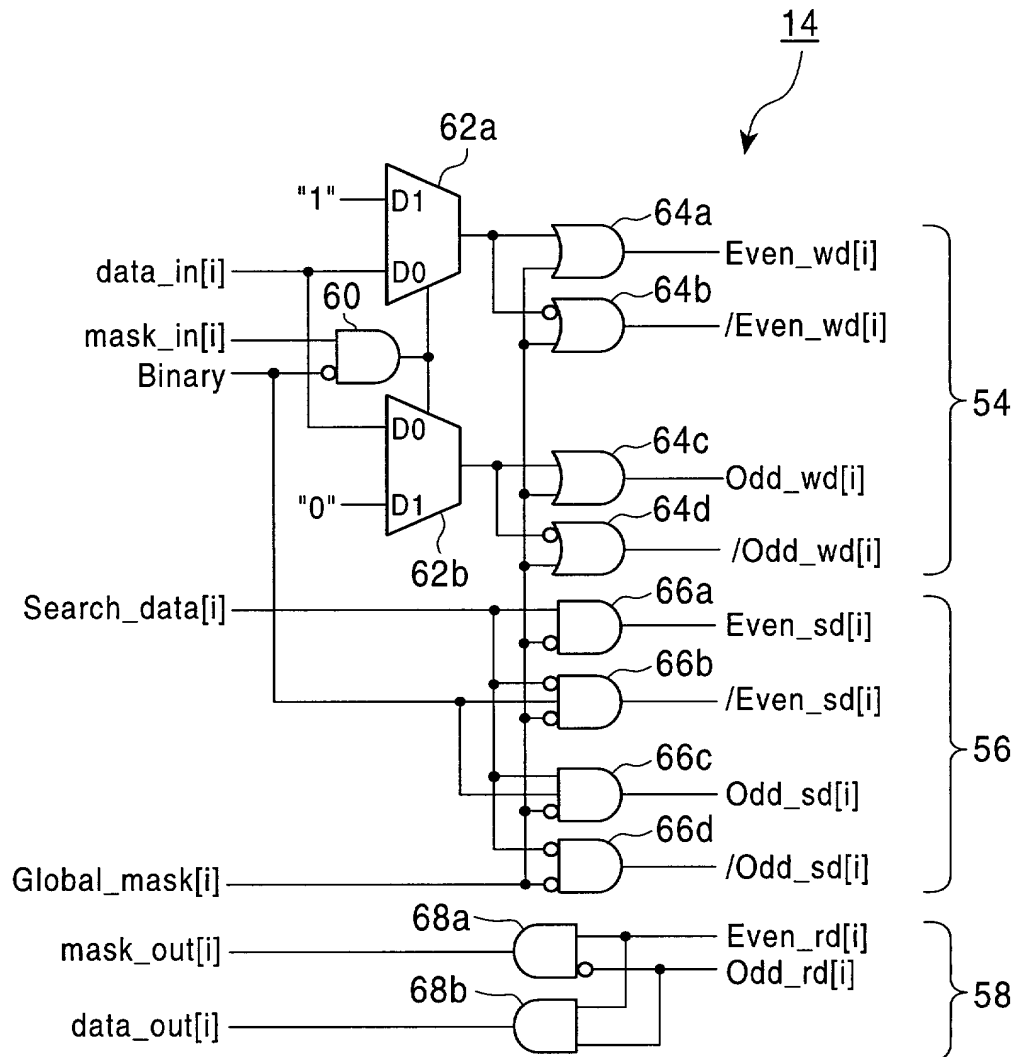


FIG. 7

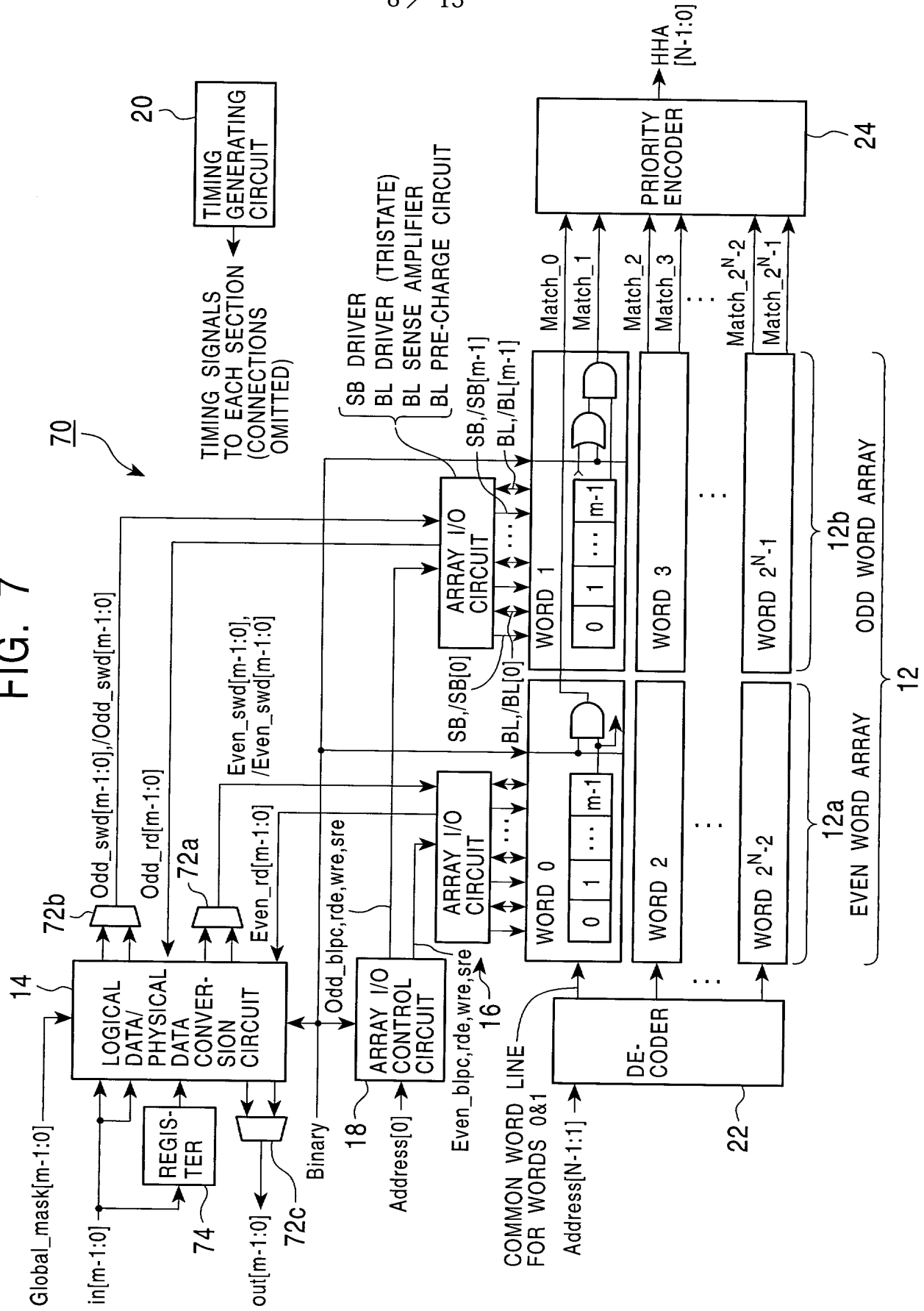




FIG. 8

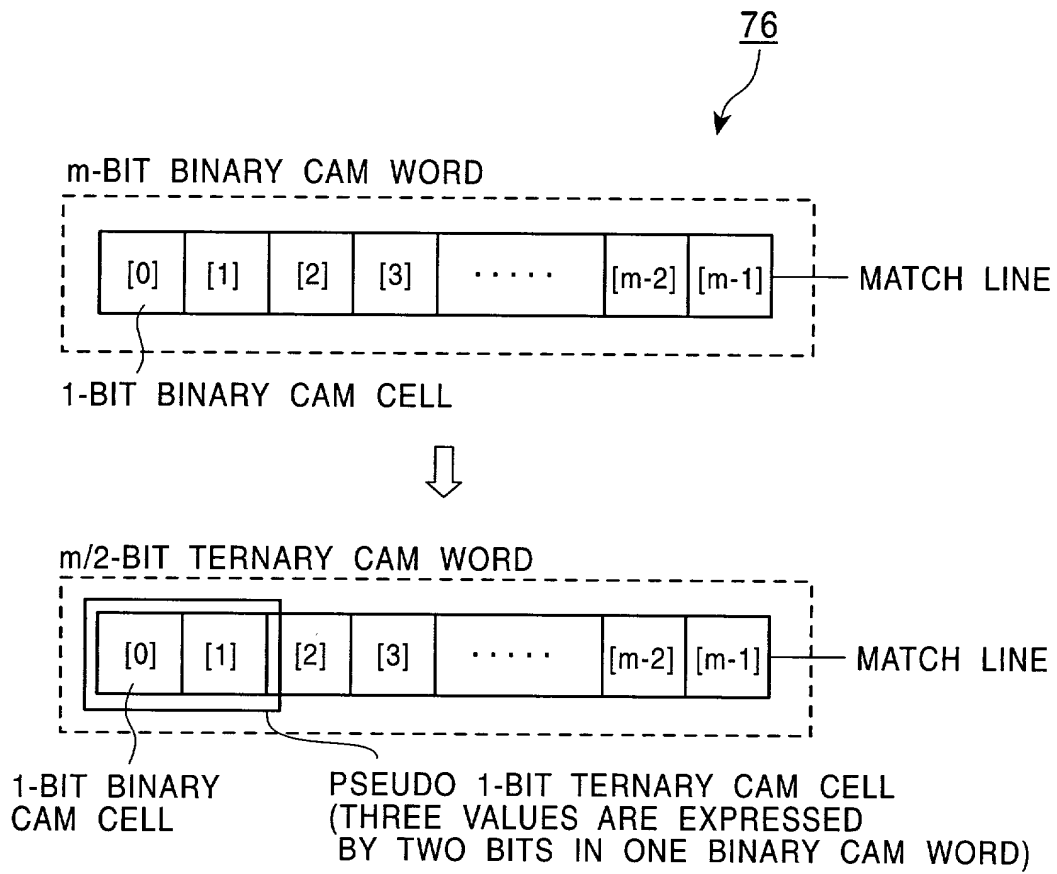


FIG. 9

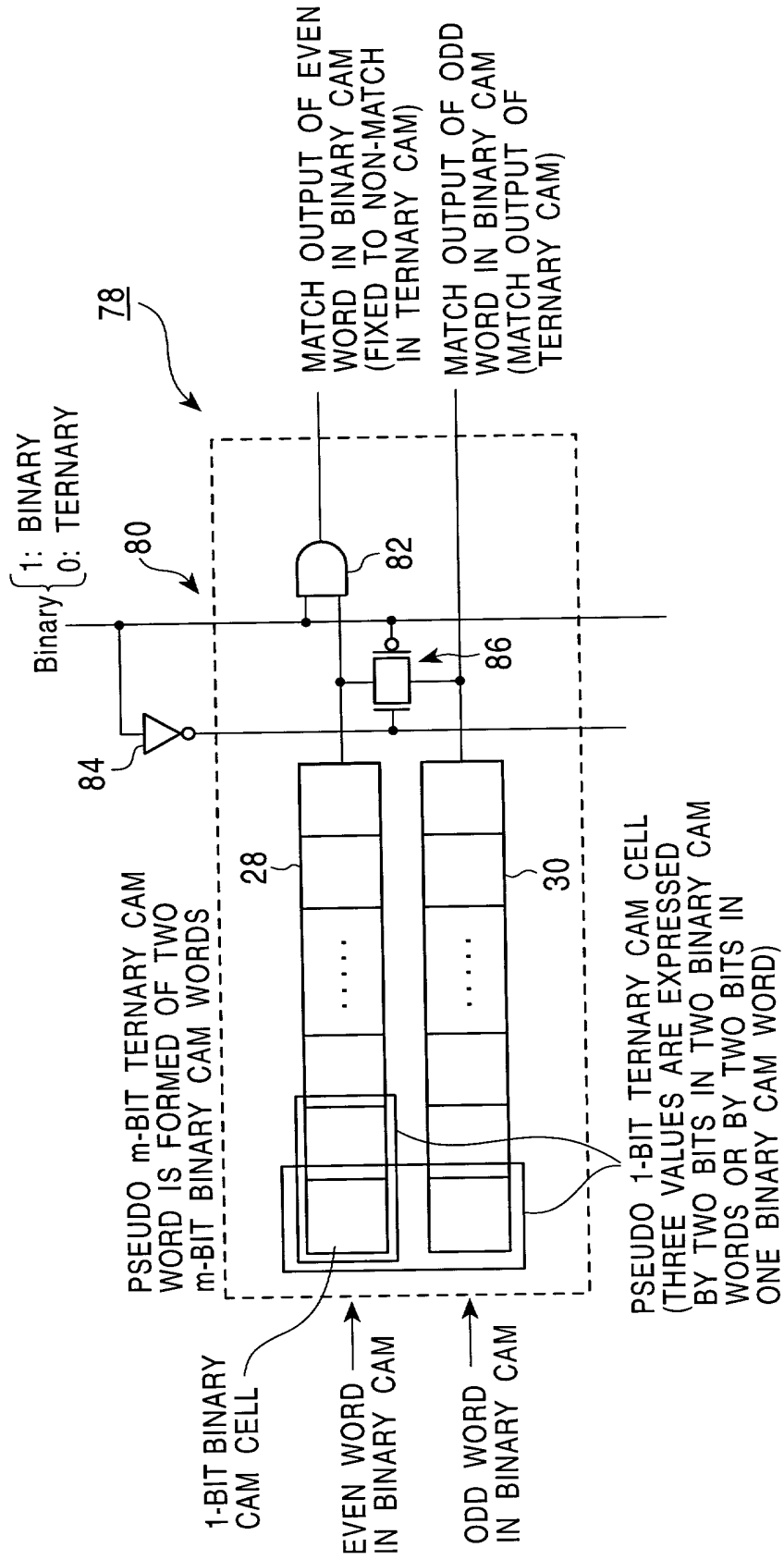


FIG. 10  
PRIOR ART

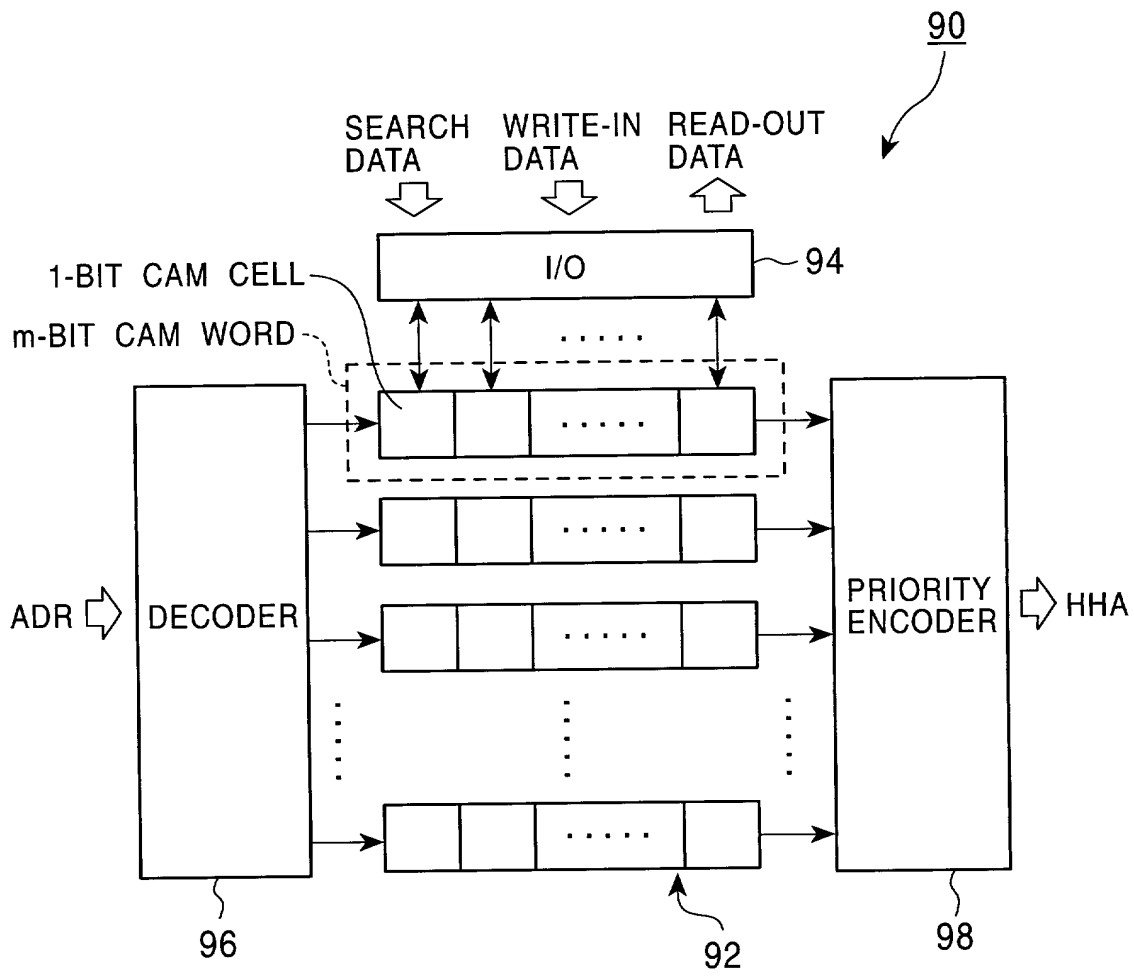
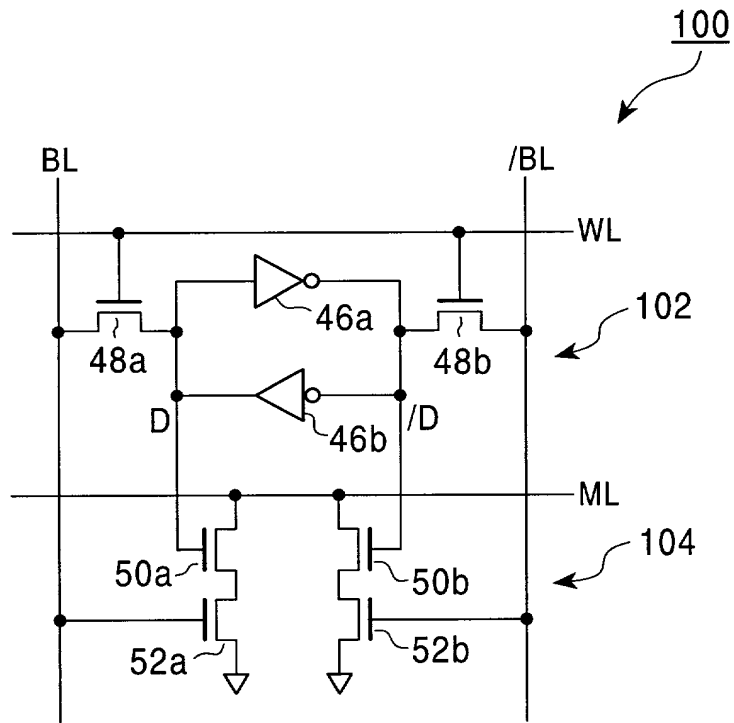


FIG. 11  
PRIOR ART



The diagram illustrates a 1T1R1C1 memory cell (106) with the following components and connections:

- Access Transistor (102):** Consists of two PMOS transistors (48a, 48b) and two NMOS transistors (50a, 50b). Transistors 48a and 50a are connected to the bit line (BL), while 48b and 50b are connected to the complementary bit line (/BL). The gates of 48a and 50a are connected to the data word line (DWL), and the gates of 48b and 50b are connected to the complementary data word line (/DWL).
- Storage Capacitor (110):** A capacitor (116) is connected between the nodes D and /D.
- Sense Amplifier (108):** Consists of two NMOS transistors (52a, 52b) and two PMOS transistors (112a, 112b). Transistors 52a and 112a are connected to node D, while 52b and 112b are connected to node /D. The gates of 52a and 112a are connected to the memory word line (MWL), and the gates of 52b and 112b are connected to the complementary memory word line (/MWL).
- Output Nodes:** The sense amplifier outputs are labeled M and /M, which are connected to the bit line (BL) and complementary bit line (/BL) through PMOS transistors 114a and 114b, respectively.